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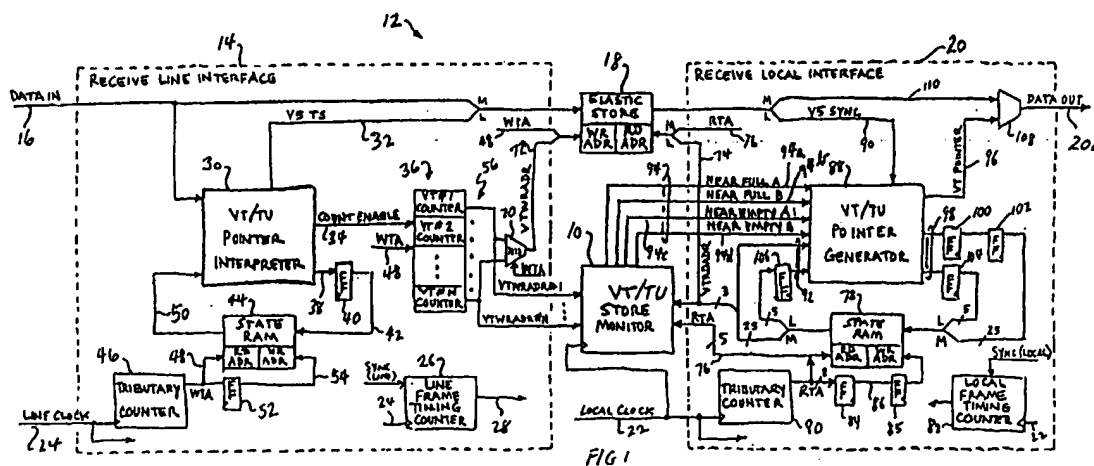
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**(54) Tributary ambiguity resolution for elastic store control.**

57 Read and write addresses on the local and line sides of an elastic store are compared at least twice in order to determine any ambiguity in the compari-

son and, if so determined, forgoing any pointer adjustments that would otherwise have been made.



## Technical Field

This invention relates to fiberoptic telecommunication transmission systems and, more particularly, to a synchronous optical network SDH element.

## Background of the Invention

An elastic store function for pre-SDH signals is known as a data buffer that is written into by one clock and read from by another. If long or short-term instabilities exist in either clock, the elastic store absorbs the differences in the amount of data transmitted and the amount of data received. Such an elastic store can compensate only for short-term instabilities that produce a limited difference in the amounts of data transmitted and received. If sustained clock offsets exist, as with highly accurate but unsynchronized clocks, an elastic store will eventually overflow or underflow. Ways to insure that overflows do not occur may involve "loop timing," where the line clock on the incoming link of a switch is nominally synchronized to the switch clock where, in essence, the inlets and outlets operate as though directly connected to each other using a common source of timing; and a "regenerative repeater" which establishes transmit timing directly from the locally derived sample clock and the long-term frequency of the transmit clock is controlled by maintaining a certain "average level of storage" in the elastic store.

In SDH systems, on the other hand, within certain constraints regarding the accuracy of the network and network element clocks, the read timing and write timing on opposite sides of an elastic store may be asynchronous. Moreover, by the use of pointers within each frame, a payload may overlap different frames and may move with respect to those frames. Thus, the SDH elastic store presents new opportunities and new problems to solve in control thereof. In particular, we recognized an ambiguity problem in SDH systems in comparing the write and read addresses provided to an elastic store.

## Disclosure of Invention

The object of the present invention is to provide a means and method for controlling a tributary elastic store without ambiguity.

According to the present invention, a tributary read or write address is made stable for more than one byte so that it may be compared, respectively, with a write or read address more than once, for the purpose of deciding whether or not an ambiguity exists; if an ambiguity is determined to exist, any pointer adjustment that would otherwise have

been made in the absence of an ambiguity, will not be made.

In an embodiment shown herein, the write side, i.e., the line side of a tributary elastic store and store monitor is equipped with separate counters for each tributary so that the address of the particular byte being stored for a particular tributary is available during the time slots associated with other VTs. Each counter provides a hard-wired write address, for the particular byte in the different tributaries being addressed, to a virtual tributary (VT)/tributary unit (TU) elastic store monitor. Only the outputs of one of these counters at a time is actually utilized as a VT write address by the elastic store itself for storing the incoming data. This address selection is done by means of a multiplexer. The VT/TU elastic store monitor, on the other hand, according to the present invention, has all of the VT write addresses available at its inputs for much more than one clock period and thus may be consulted for comparison purposes with the read address more than once in successive bytes.

In further accord with the present invention, the comparison between the write address and the read address is carried out at least twice in order to detect ambiguities in the comparison. In an embodiment shown below, the comparison consists of a subtraction operation performed twice to filter possible "glitches" on the detected signals. In still further accord with the present invention, by providing a write counter that stays stable for a plurality of clock periods, e.g., twenty-eight clock periods for a VT 1.5 structured SPE, the counters on the other side may be designed as a single counter and counts can be stored in a time division multiplexed VT/TU pointer generator state RAM. The first comparison between the read and write counters will not necessarily be reliable because of the phase difference between the line and network element rate clocks and therefore, according to the present invention, filtering is required. Holding the read counter value at least one more byte period and performing another comparison will provide an accurate decision for pointer adjustments.

According to an embodiment of the present invention, for VT 1.5 tributaries, a twenty-eight VT pointer processor shares the same RAM as an elastic store as well as pointer processor circuits.

A near empty or a near full decision is given depending on the position of the elastic store read and write counters. Elastic store RAM is partitioned for a twenty-eight VT payload which requires twenty-eight read and twenty-eight write counters. A novel time division multiplexed pointer processing method allows us to use only one pointer processor circuit for all twenty-eight VTs, excluding elastic store write counters. The read counter is

selected to be time shared between twenty-eight VTs. The elastic store control circuit subtracts the write counter value from the read counter value and also latches the read counter outputs which will contain the read addresses of the same VT in the next clock period which could be the next VT. The subtraction is performed one more time to detect a possible difference in the detected signals.

These and other objects, features and advantages of the present invention will become more apparent in light of a detailed description of an embodiment thereof, as illustrated in the accompanying drawing.

#### Brief Description of the Drawing

Fig. 1 shows a receive section of a SDH network element, according to the present invention, having an elastic store and a store monitor in between a receive line interface running at a line clock rate and a receive local interface running at the same rate by means of a local clock wherein there will typically be a phase difference and slight frequency differences between the line and local clocks.

Fig. 2 shows a method, according to the present invention, for resolving ambiguities which may exist because of the asynchronous relation between elastic store write timing on the line interface side and elastic store read timing on the local side.

Fig. 3 shows a stable write address twice compared, at two different times, to asynchronous read addresses, one without ambiguity and one with.

Fig. 4 shows a read-write address comparison part of a VT 1.5 elastic store monitor block of Fig. 1 in detail, according to the present invention.

#### Best Mode for Carrying Out the Invention

Fig. 1 shows a virtual tributary (VT)/tributary unit (TU) elastic store monitor 10, according to the present invention, as part of a receive section 12 of a synchronous optical network element also having a receive line interface 14 responsive to incoming serial data on a line 16 for storing such data in an elastic store 18, a receive local interface 20 for reading out such stored data from the elastic store 18 and providing same on a line 20a at a local clock 22 rate as controlled by the monitor 10.

A line rate clock on a line 24 is extracted from the incoming data on the line 16 and used throughout the receive line interface by various synchronous devices including a line frame timing counter 26 responsive to line sync and clock signals for providing a synchronization and timing signal on a line 28 for line side devices within the interface 14. A VT/TU pointer interpreter 30 is responsive to the

incoming data on the line 16 for detecting pointers and interpreting same.

The pointer interpreter 30 provides a synchronization signal on a line 32 to the elastic store 18 and a count enable signal on a line 34 to a plurality of VT/TU counters 36. It also provides a VT/TU pointer state signal on a line 38 to a flip-flop 40 where it is stored for one line clock cycle and then provided on a line 42 to a state memory 44, which is a dual-port random access memory (RAM), where it may be stored for a passage of time until the same VT time slots reoccur. Thus, a particular VT will have the last state of its pointer interpretation stored in the state RAM 44 for the period of time required to process other tributaries. A tributary counter 46 provides a write tributary address (WTA) signal on a line 48 to the state RAM 44 for reading previous state data out on a line 50 to the pointer interpreter 30 and also to a flip-flop 52 for delaying the read (WTA) address by one line clock for providing the write address on a line 54 to the state RAM 44 for writing the state information on the line 42 into the state RAM 44.

The write tributary address signal on the line 48 is also used by the multiplexer 70 to output one VT elastic store write address at a time. The VT counters 36 provide a plurality of count signals on lines 56 to the VT/TU store monitor 10. The reason for having a plurality of counters is to be able to provide stable addresses for comparison purposes with the read addresses, on the local side, which go by much more quickly. Thus, referring to Fig. 2-(a) it will be observed that the WTA signal which is shown for a VT 6 structure, for example, provides a new VT address seven consecutive clock periods. It should be noted that the frame boundaries are not shown because they have no fixed relation (at least in the VT floating mode) to the beginning of the VT payload. In Fig. 2(b) the elastic store write address for VT number one is shown being held by VT number one counter until the same VT is processed next time in order to provide a stable reference for the VT/TU store monitor, for the purpose of helping in discerning ambiguities. Similarly, in Fig. 2(c) VT write address number two which begins at the beginning of the next VT is held on appropriate lines of the lines 56 until the new byte of the same VT. Therefore, it will be observed from Fig. 2(a), (b) and (c) that even though the write tributary address on the line 48 is being changed every time a new VT begins to be processed, the VT counters 36 will hold a newly addressed VT's address for allowing access for more than one VT period to the VT/TU store monitor 10.

A multiplexer 70 provides a selected VT write address on a line 72 which is combined with the WTA signal on the line 48 in order to properly address the elastic store 18 for storing the incom-

ing data 16 at the proper time according to the V5 sync signal on the line 32.

The stored data and V5 pointer are read out of the elastic store 18 by a VT read address signal on a line 74 as combined with a read tributary address (RTA) signal on a line 76. The VT address signal on the line 74 is provided by a state RAM 78 in response to the RTA signal on the line 76 as provided by a tributary counter 80 as driven by the local clock 22. Local frame timing is provided by a counter 82 in response to the local clock and synchronization (frame and multiframe) signals which provides synchronization and timing for devices of the local interface 20. A pair of flip-flops 84, 85 provide a two clock delay between the RTA provided to the read address function of the state RAM 78 and a write address function as addressed by a delayed read tributary address signal on a line 86.

A VT/TU pointer generator 88 is responsive to a V5 synch signal on a line 90 which is read out of the elastic store 18, and is responsive to a plurality of previous state signals on lines 92 provided by the state RAM 78 and is responsive to a plurality of near full and near empty signals on lines 94 for providing a VT pointer signal on a line 96 and for providing a plurality of next state signals on lines 98 for storage in the state RAM 78. A plurality of flip-flops 100, 102, 104, 106 are placed in the signal path between the VT/TU pointer generator 88 and the state RAM for the purpose of compensating for delays created elsewhere in the circuit.

The incoming data signal on line 16 is thus read into the elastic store 18 at the line clock 24 rate and read out in the receive local interface 20a at the local clock 22 rate. The data on line 20 is from a multiplexer 108 which combines both the pure data on a line 110 read from the elastic store 18 with the VT pointer, with adjustments, on the line 96. The adjustments in the VT pointer on line 96 permit the VT/TUs to "float" with respect to the frame. Referring back to Fig. 2, in Fig. 2(d), the VT read address signal on the line 74 of Fig. 1 is shown being provided every time a new VT needs to be read out. The three bits making up this signal do not identify the particular VT. That particular information is provided by the RTA signal as shown in Fig. 2(e). It is noted that a common time line is shared between of Figs. 2(a)-(e) and therefore it will be observed that the alignment of the VTs, as written into the elastic store, do not always correspond in the same relation to the timing of the read operation of the same VT on the same read side. Thus, read timing is asynchronous to write timing, as indicated in Fig. 2(e), and they may drift in one direction or slide back and forth with respect to one another.

Inasmuch as the write side has been chosen to provide the stable reference address by means of the counters 36, the comparison operation carried out by the elastic store monitor 10 is carried out by reference to the read addresses. Thus, in Fig. 2, the checking of VT number one is done right after the reading of VT number one is completed on the receive local interface 20 side as shown by a comparison line 109 extending between Figs. 2(b) and 2(e). Since, as shown in Fig. 2(b), the VT write address corresponding to VT write address number one is being stored in the VT number one counter for a lengthy period in counters block 36 on the line side 14, the correspondence between the read address and the write address may be checked more than once (at times A and B). The reason for wanting to check the correspondence between the read address and the write address more than once is that there may be an ambiguity near the boundaries due to the asynchronous relationship between read and write timing. As shown in Fig. 3, if two comparisons of a read address as shown in Fig. 3(b) are done well after and well before the change of the write address of Fig. 3(a), there will be no ambiguity indicated. However, from time to time, a comparison will be done as shown in Fig. 3-(c), where the read-write comparison will yield different results. Thus, the present invention first seeks to determine if there is an ambiguity between successive comparisons and, if such ambiguity is detected, then any pointer adjustments which would otherwise have been made are prevented until the ambiguity is resolved. Thus, if the ambiguity persists there will be no further pointer adjustments. If the ambiguity goes away after one or more successive checks, then pointer adjustments may thenceforth be freely made.

In the illustration shown in Fig. 2, the checking is shown taking place in the middle of the counter holding period. However, eventually the checking process will reach a boundary as indicated in Figs. 3(a) and (c) at which point there may be a difference between the two comparisons of the write and read addresses. Thus, if there is such a difference detected between the two comparisons, then any pointer adjustments that would have otherwise been made will not be made until the difference disappears in future comparisons. Thus, if there is an indication that either of these comparisons do not result in the same difference then no pointer adjustments will be allowed in the pointer generator 88.

Referring now to Fig. 4, a VT elastic store ambiguity monitoring function is shown, according to the present invention. A 3-bit multiplexer 130 multiplexes twenty-eight VT write counter addresses on the line 56 (see Fig. 1) as controlled by the five most significant bits of an eight bit VT read

address on the line 76 (see Fig. 1). The three bit multiplexer 130 provides a selected VT write address on a line 132 for comparison with the three least significant bits of the VT read address signal on the line 74 (see Fig. 1). A three-bit subtractor decoder 134 is responsive to the VT write address signal on the line 132 and the three-bit VT read address on the line 74 for comparing the two according to an algorithm that will produce a near full or near empty signal if the absolute difference becomes greater than a selected limit, depending on the size of the elastic store 18. In the example, the elastic store has eight bytes available for storage purposes and the near full and near empty signals will be provided within two bytes of the limits of the eight byte space. In any event, the three-bit subtractor decoder will either provide no indication of a need for an adjustment, a near full signal on a line 136 or a near empty signal on a line 138. Each of the signals 136, 138 are stored in flip-flops 140, 142, respectively.

Thus, referring back to Fig. 2, the comparison made in the subtractor decoder 134 might be thought of, by way of example, as corresponding to the check indicated by the line 109 of VT number one taking place in Fig. 2(b) at point A after the read address for tributary one is finished. The difference would be two bytes and, although not shown as such in the Figure, it may be assumed for purposes of illustration that the read addresses of Fig. 2(d) are ahead of the write addresses of Fig. 2(b) in time, and the difference will represent a near full condition and therefore the signal on the line 136 will be provided to the flip-flop 140.

At the end of the very next tributary, i.e., tributary two as read on the local interface 20 side, a three bit multiplexer 150 will select the address of tributary number two in the VT counters 36 of Fig. 1 as selected by the same signal previously provided in the previous VT to the three bit multiplexer 130. A flip-flop 152 has stored the VT read address on the lines 74, 76 for one VT period. Unless a boundary 154, as shown in Fig. 2(b), has occurred between the A and B readings, there should still be the same difference between the signal on a line 156 and a line 158 to a decoder subtractor 160, as before. Thus, a near full signal on a line 162 will be active indicating a near full condition, as before, and a near empty signal on a line 164 will be inactive. A near full signal on a line 166 will be active, having been previously stored in the flip-flop 140 during the last check. Similarly, a near empty signal on a line 168 will be inactive.

Since the signals on lines 162, 166 are both present, indicating there is no ambiguity between the two subtractions carried out by the subtractors 134, 160, an AND gate 170 will provide a VT near full signal on a line 172. Similarly, if the compari-

son had indicated a near empty condition for both subtractions, an AND gate 174 would have provided a near empty signal on a line 176. If either of these signals on the lines 172, 176 are present, then no ambiguity exists and any pointer adjustments indicated by the magnitudes thereof are permitted to go forward in the VT/TU pointer generator 88 of Fig. 1. The and gates 170, 174 may be located in the elastic store monitor 10 or the VT/TU pointer generator 88. In the actual embodiment that we carried out, the AND gates 170, 174 were outside the actual VT elastic store monitor so we show the lines 94 in Fig. 1 before going into the AND gates which may be presumed in this case to be inside the generator 88 in Fig. 1.

Although the invention has been shown and described with respect to a best mode embodiment thereof, it should be understood by those skilled in the art that the foregoing and various other changes, omissions and additions in the form and detail thereof may be made therein without departing from the spirit and scope of the invention.

#### Claims

##### 1. An elastic store ambiguity detector, comprising:

a first comparator (134), responsive to a read address signal (74) and a write address signal (132), for providing a first near full signal (136) and a first near empty signal (138);

first storage means (140, 142), responsive to the first near full and first near empty signals and to a clock signal, for storing the first near full and first near empty signals for a clock period and for providing a delayed first near full signal (94c) and delayed first near empty signal (94d) after the clock period;

second storage means (152), responsive to the clock signal and to the read address signal (74), for storing the read address signal for the clock period and for providing a read address signal (158) after the clock period;

a second comparator (160), responsive to the read address signals (158) provided by the second storage means (152) and to a write address signal (156), for providing a second near full signal (94a) and a second near empty signal (94c);

means (170), responsive to the first near full signal (94c) and the second near full signal (94a), for providing a confirmed near full signal (172) only in the presence of both first and second near full signals (94a, 94c); and

means (174), responsive to the second near empty signal (94d) and the first near empty signal (94c), for providing a confirmed near empty signal (176) only in the presence

of both first and second near empty signals (94c, 94d).

2. A pointer processing method, comprising the steps of:
- comparing, in two successive steps, a write address with a read address provided for an elastic store, for providing a pointer adjustment enable signal if said comparing steps determine an identical comparison in the two comparing steps and the comparison has a magnitude indicative of a near full or a near empty condition of said elastic store; and
  - allowing a pointer adjustment in the presence of said enable signal.
3. A pointer processing method, comprising the steps of:
- comparing, in successive steps, a write address with a read address provided for an elastic store, for failing to provide a pointer adjustment enable signal if said comparing steps determine a disagreement in the comparing steps; and
  - disallowing a pointer adjustment without said enable signal being provided.

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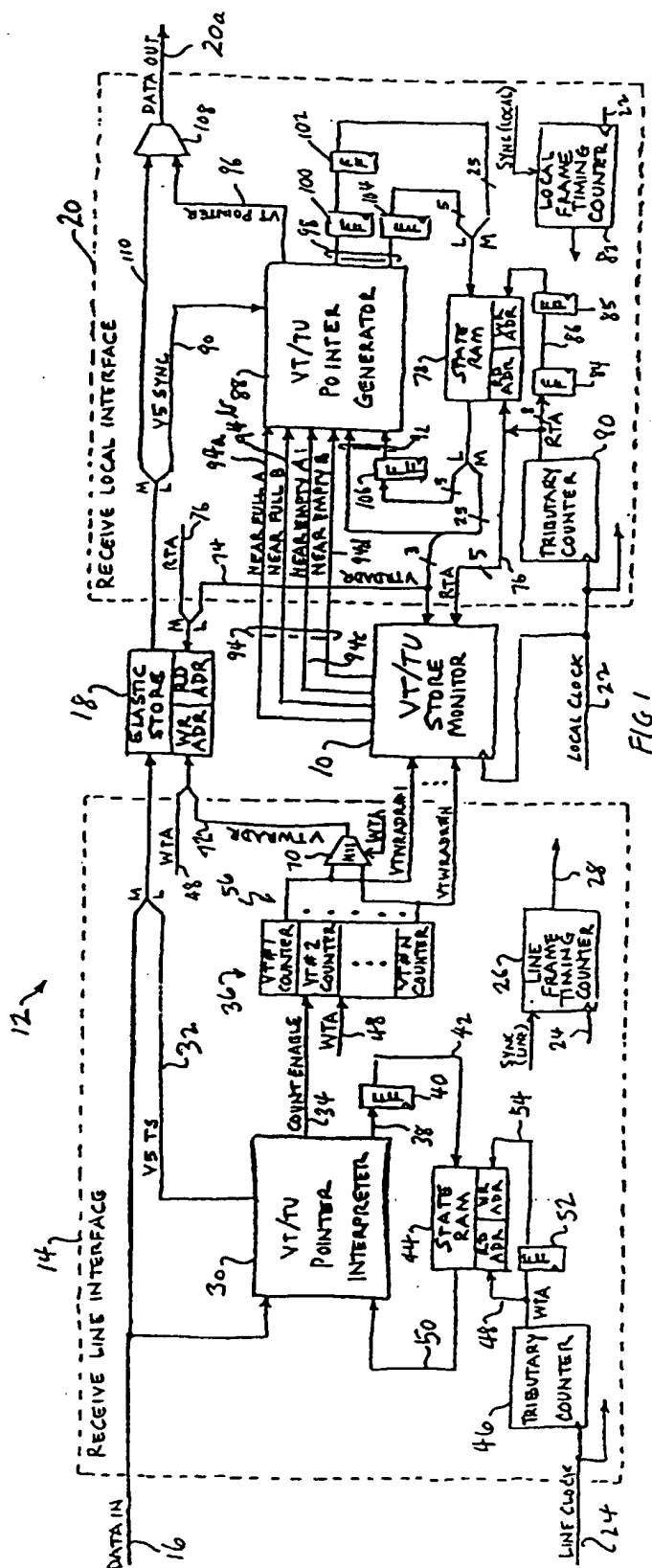
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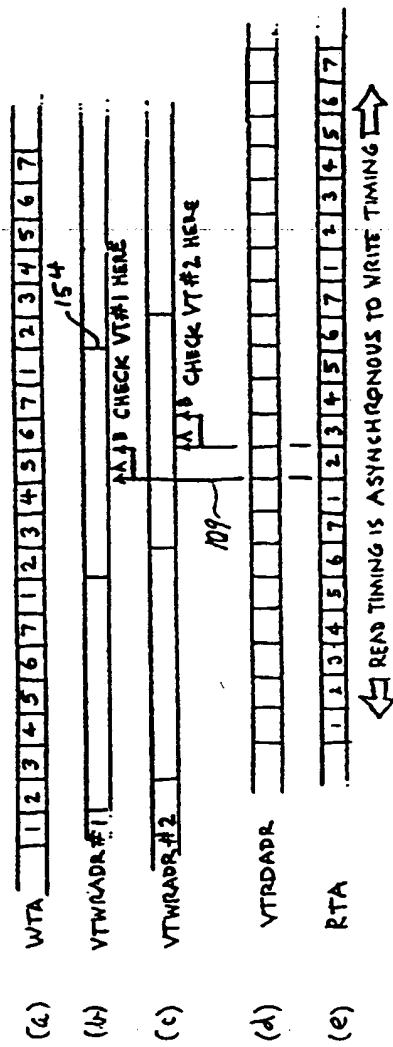


FIG 2

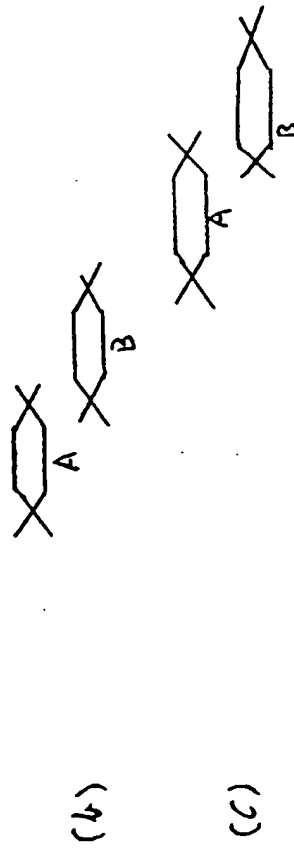


FIG 3

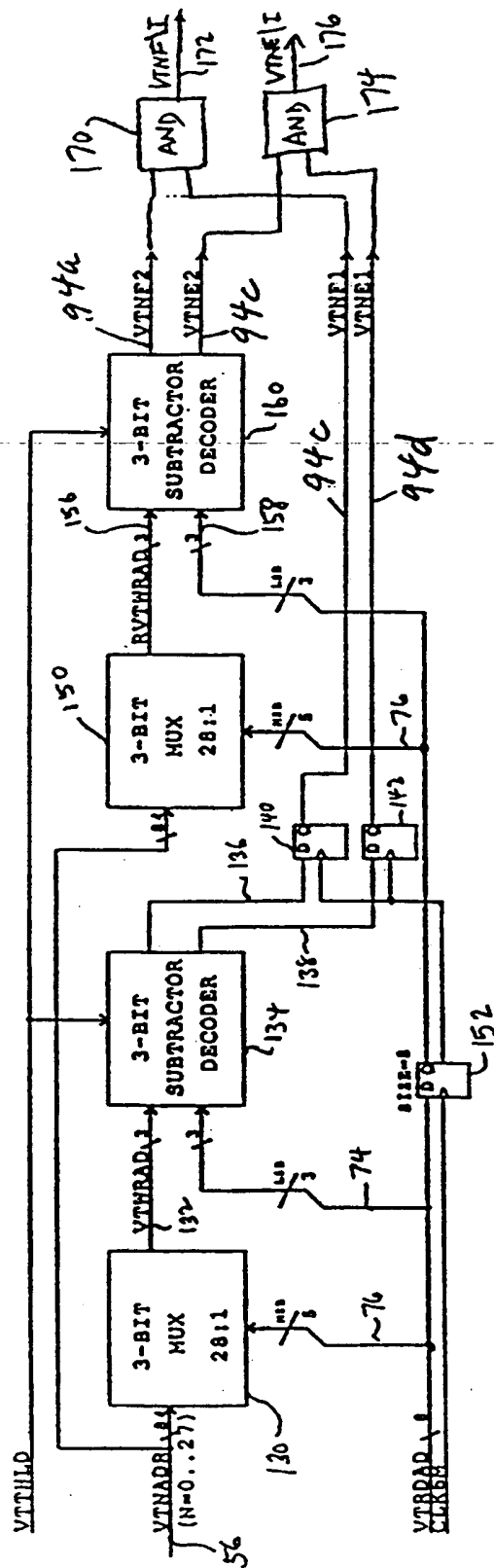


FIG-4



European Patent  
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## EUROPEAN SEARCH REPORT

Application Number

EP 93 10 7959

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	WO-A-9 202 999 (TRANSWITCH) * page 8, paragraph 2 - page 13, paragraph 2; figures 6,7 *	1-3	H04J3/06 G06F5/06
A	--- PROCEEDINGS OF THE IEEE 1989 CUSTOM INTEGRATED CIRCUITS CONFERENCE 15 May 1989, SAN DIEGO, US pages 23.4.1 - 23.4.4 M. KAWAUCHI ET AL. 'A 1.0um Compilable FIFO Buffer for Standard Cell' * page 23.4.1, right column, paragraph 2; figures 1-3 *	1-3	
A	--- IRE WESCON CONFERENCE RECORD vol. 33, November 1989, NORTH HOLLYWOOD US pages 120 - 124 M. SHAMSHIRIAN 'HIGH DENSITY PROGRAMMABLE FIFOs ADD DESIGN FLEXIBILITY' * page 121, left column, paragraph 2; figure 1 *	1-3	
A	--- EP-A-0 226 017 (IBM) * column 9, line 17 - column 13, line 18; figure 4 *	1-3	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A	--- WO-A-9 004 294 (DIGITAL EQUIPMENT CORP.) * abstract * * page 33, paragraph 3 - page 35, paragraph 2; figures 1,6 *	1-3	H04J G06F
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 18 AUGUST 1993	Examiner PIEPER T.
<b>CATEGORY OF CITED DOCUMENTS</b> X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

